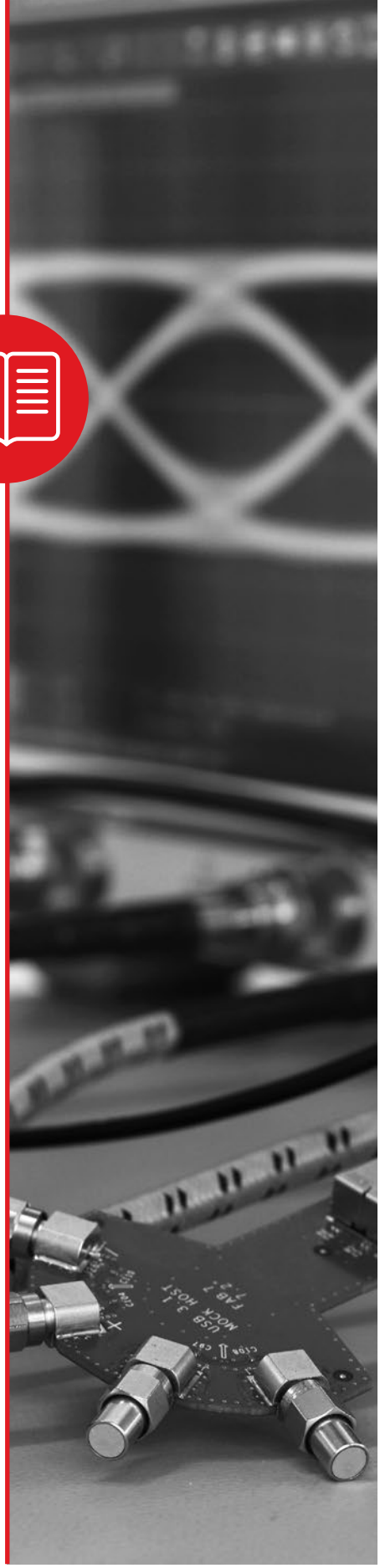
WHITE PAPER

SIGNAL INTEGRITY FOR HIGH-SPEED DATA TRANSMISSION, CHALLENGES AND SOLUTIONS

EDITION 1.0 | DECEMBER 2021



Fischer CONNECTORS

REIMAGINING CONNECTIVITY TOGETHER

INTRODUCTION

Requirements for high-speed data transmission, the need for ever greater bandwidth and drastically increasing design complexity present new challenges to design engineers. This document aims to help engineers optimize their products. It explains high-speed data transmission protocols, where problems may arise, and how to design connectors for high-speed data transmission. It also covers suitable test methods and system-level testing.

MOHAMMAD AZADIFAR
Signal Integrity Engineer, Fischer Connectors

Mohammad Azadifar is Fischer Connectors' Signals expert. Holder of a PhD in Electrical and Electronics Engineering from EPFL (the Swiss Federal Institute of Technology in Lausanne), Mohammad is a Senior Member of IEEE (the Institute of Electrical and Electronics Engineers) – the world's largest technical professional organization for the advancement of technology. Mohammad has contributed technical articles to IEEE on research topics such as Computational Electromagnetics, Lightning Physics, Metamaterials and Time Reversal Imaging. In the Fischer Connectors Group's R&D center, he provides his extensive experience in signal integrity engineering to advance connectivity technology in various high-speed data transmission and EMI/EMC projects.

INDEX

THE CONNECTIVITY MATTER

The emergence of high-speed data transmission during the past decades and the demand for greater bandwidth during the coming years are driving engineers in each part of the connectivity system, from software developers to cable-connector providers, to optimize their products while ensuring they meet the new requirements.

As technology evolves, high-speed interconnect phenomena that designers have historically ignored have begun to dominate performance, and unforeseen problems have arisen that drastically increase the complexity of design.

As the maximum required frequency (fmax) of a signal goes high compared to the distance that it needs to travel, simplified lumped circuit models must be replaced with their high-frequency counterparts, such as transmission line formulation or even full wave Maxwell's equations [1]. Hence, DC connectivity of metallic surfaces can no longer guarantee high-speed connectivity.

FIG.1

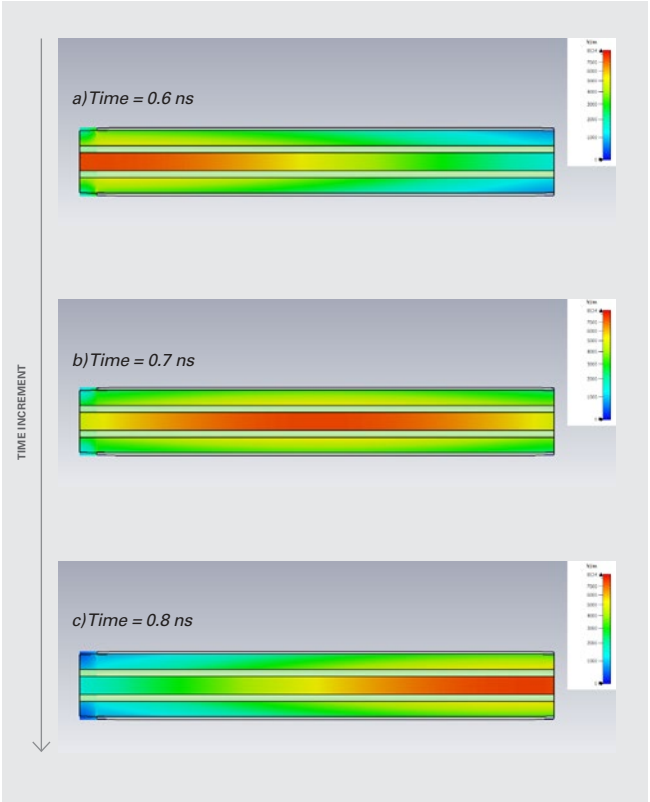


Figure 1. Energy transport in a simplified connector from one side to the other side. Connectivity is not only provided via metallic conduction but also via dielectric polarization.

Figure 1a to 1c shows an example of such a phenomenon. We can observe that the transport of energy from one side of a connector to the other side at three instances of 0.6, 0.7, and 0.8 ns manifests the wave propagation via polarization field.

Any geometrical entities can potentially improve or disturb the flow of energy. Hence, every high-speed related design must be cross optimized for all aspects of Mechanical, Electrical, Signal Integrity, and EMI/EMC performances.

In Figure 2, we show what happens for an analog signal passing from one side of a cable-connector solution to the other side. Reflections and attenuation are the two main mechanisms of signal degradation. Apart from these two effects, noise and crosstalk by other pairs are other parameters that can cause problems.

Let us first discuss what happens at the intersection of the transmitter and connector. If the input impedance of the transmitter is different from the input impedance of the connector, part of the input energy will reflect towards the transmitter (red arrow). Some of the remaining energy will be lost in the connector due to metallic or dielectric loss, and the wave will reach the other side of the connector. A phenomenon similar to that described above will occur at this interface.

However, reflection losses are the most important mechanism of loss of signal at the connector; attenuation (insertion loss) is the main mechanism of loss in the cable itself.

FIG.2

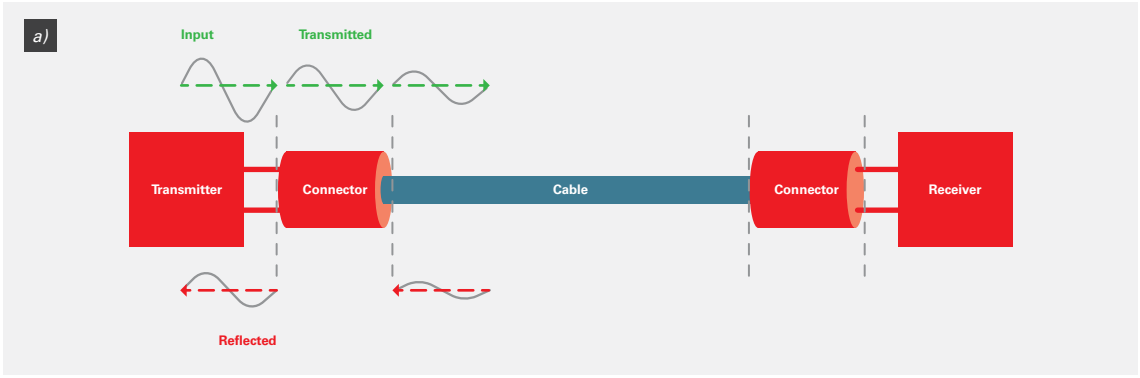


FIG.3

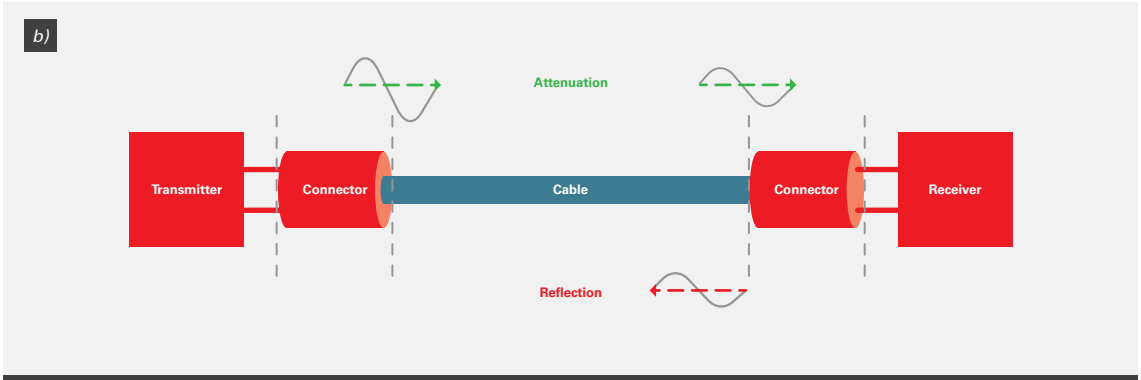


Figure 3. Signal degradation due to attenuation and impedance mismatch: a) on the transmitter side, b) on the cable and receiver side.

We have discussed qualitatively the problem of analog signal propagation in the cable-connector. Now we can use the Fourier transform and superposition principle to study the behavior of digital signal propagation. In another words, what happens to a digital signal is the summation of what happens to its harmonics. An example of digital signal degradation is shown in Figure 4.

It is worth mentioning that the overall speed of a link is also a function of transmitter and receiver performances. One can have the best cable and a bad transmitter and still not reach the full speed, and vice versa. For example, in USB3 specifications, many requirements focus on transmitter and receiver specifications. Hence answering the question of 'what is the speed of data transmission for only a cable and a connector' is a challenging task. We will further discuss this matter in Section 5, by reviewing the concept of system-level analysis.

FIG.4

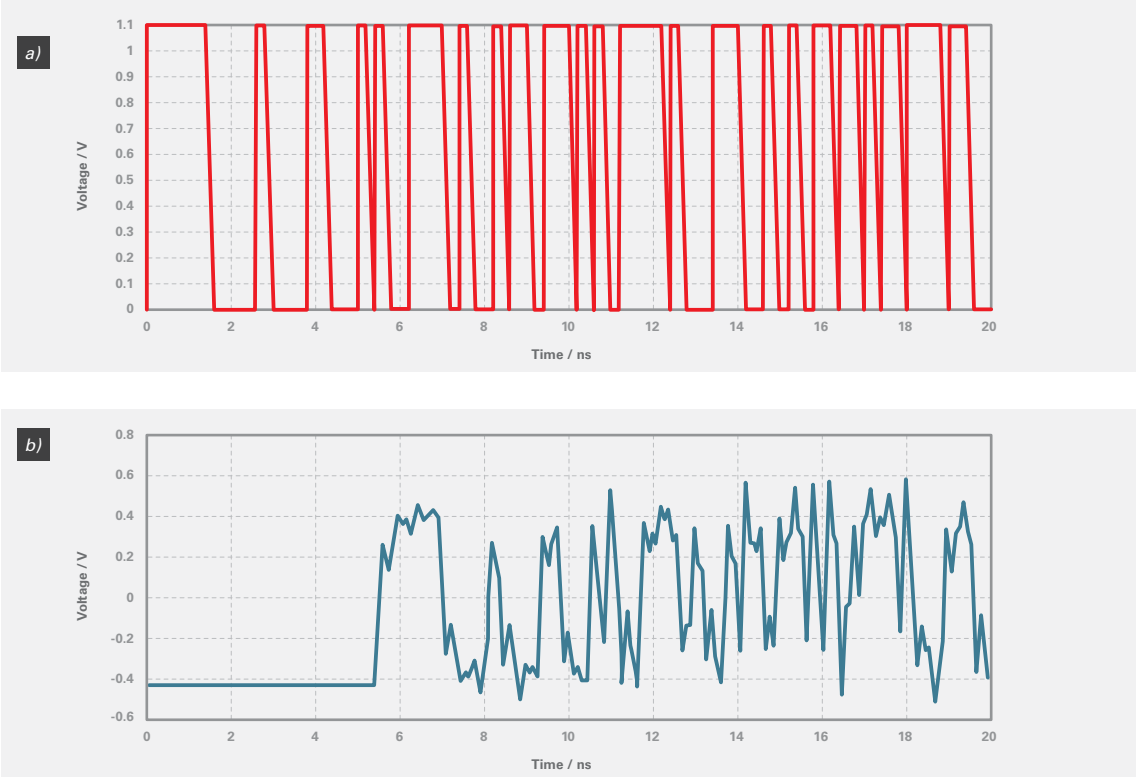


Figure 4. Waveform degradation of digital 5 Gbps signals: a) ideal input PBRS, b) received at receiver input.

HIGH-SPEED DATA TRANSMISSION PROTOCOLS

High-speed data transmission protocols provide guidelines and specifications to describe various layers of the OSI model [2] including specifications for the physical layer, data link layer, etc. Here we focus on the specifications for cable and connector assembly of the physical layer. We will include some other parts of the physical layer in Section 5 to estimate the system-level performance.

Above the physical layer, we have the data-link layer which can detect and even correct bit errors and influence the overall user experience. Normally an overall bit error rate (BER) of 1e-12 is tolerated in the physical layer.

To achieve the required BER, standards usually specify parameters for cables and connector assembly. Some of the usual parameters required for cable-connector assembly are as follows:

- Impedance matching: ratio of V/I or E/H
- Line delay: the latency of signal propagation
- Insertion and return losses: attenuation and mismatch
- NEXT, FEXT crosstalk levels: field coupling from one channel to the other one within a cable
- Mode conversion losses: identifies the imbalance of pairs
- Shielding performances: how much we disturb others or may be disturbed
- Integrated parameters: includes the interaction of multiple parameters together

FIG.5

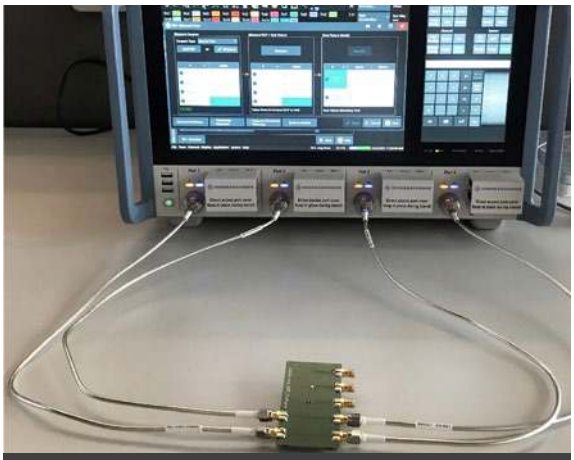


Figure 5. Vector Network Analyzer for measuring the link parameter in frequency domain.

Measurement of these parameters is usually undertaken in the frequency domain using a Vector Network Analyzer (VNA). For the impedance measurement, one can also use a Time Domain Reflectometry (TDR) device.

CONNECTOR DESIGN FOR HIGH-SPEED DATA TRANSMISSION

As discussed in Section 1, for high-speed applications the transmission line formulation dominates the transmission of signals. The main assumption in this formulation is wave propagation via Transverse Electromagnetic (TEM) modes, which has lower cut-off frequency of zero.

But once the media is excited with broadband signals, higher Transverse Electric (TE) and Transverse Magnetic (TM) modes with non-zero cut-off frequency may be excited. These modes have different phase velocities compared to TEM modes; hence their presence is unwanted. The best design practice is to have a geometrical design which shifts the cut-off of TE and TM modes to higher frequencies. An example of electric field (y-component) distribution of TEM mode is given in Figure 6, in which the x-component (not presented) is almost zero.

FIG.6

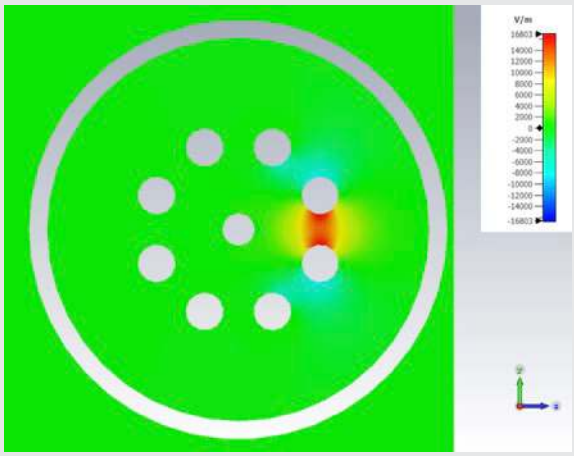


Figure 6. An example of electric field (y-component) distribution of TEM mode.

After ensuring mastery of the TEM mode of propagation by observing the longitudinal field distribution, it is essential to make sure that pin diameters and their distributions are designed properly to achieve the right impedance. An example of geometrical optimization to achieve proper impedance is shown in Figure 7. It is worth noting that the design of a connector can affect NEXT and FEXT performances, and the connector must be optimized against these constraints as well.

FIG.7

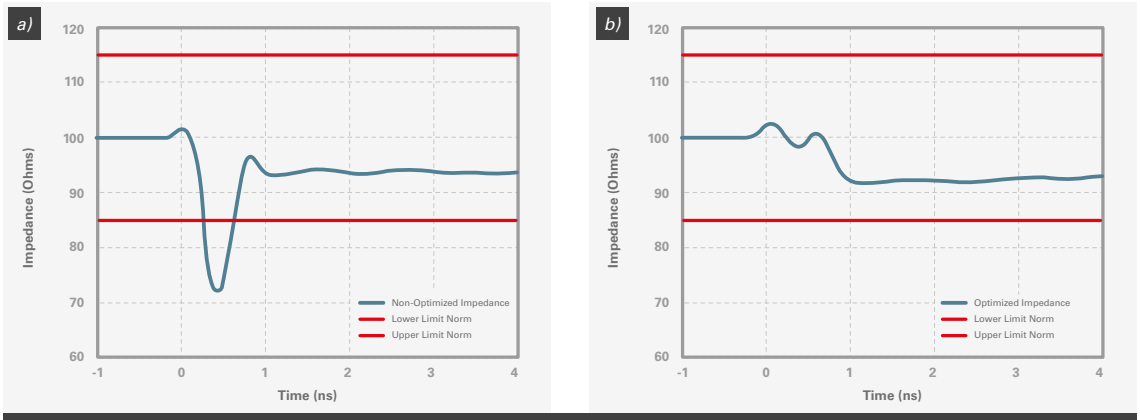


Figure 7. Measured TDR impedance response of: a) a non-optimized connector, b) an optimized connector.

HIGH-SPEED DATA TRANSMISSION TEST METHODS

As discussed in Section 2, VNA measurement is needed to obtain the frequency domain transmission parameters of the cable-connector solution. Typical devices to be tested do not have coaxial interfaces, so test fixtures are often required to be inserted between an instrument's coaxial interface and the device under test (DUT), such as a printed circuit board (PCB), package, connector, cable, etc.

To connect the cable-connector assembly to the VNA device, one needs to design a high-speed precision PCB based on the required bandwidth. In order to ensure high-quality results, one should perform the following tasks according to IEEE Std 370™-2020:

FIG.8

Figure 8. Examples of PCB fixtures for VNA measurement.

- Design PCB fixtures according to three different classes of PCBs in terms of performance (class A, B, or C)
- A proper de-embedding method must be used to remove the effect of fixtures, and quality of the de-embedding must be assured
- The quality of S-parameter results must be verified against passivity, causality and reciprocity metrics

Some examples of such fixtures are shown in Figure 8. We use the validated In-Situ De-embedding (ISD) by Ataitec with our R&S ZNB20 VNA. Examples of results are provided in Figure 9, against USB 3.2 Gen 2 specifications of Impedance, Insertion loss, NEXT of SS pairs, NEXT of SS Pair to DD Pair and Differential to Common Mode Conversion Loss.

FIG.9

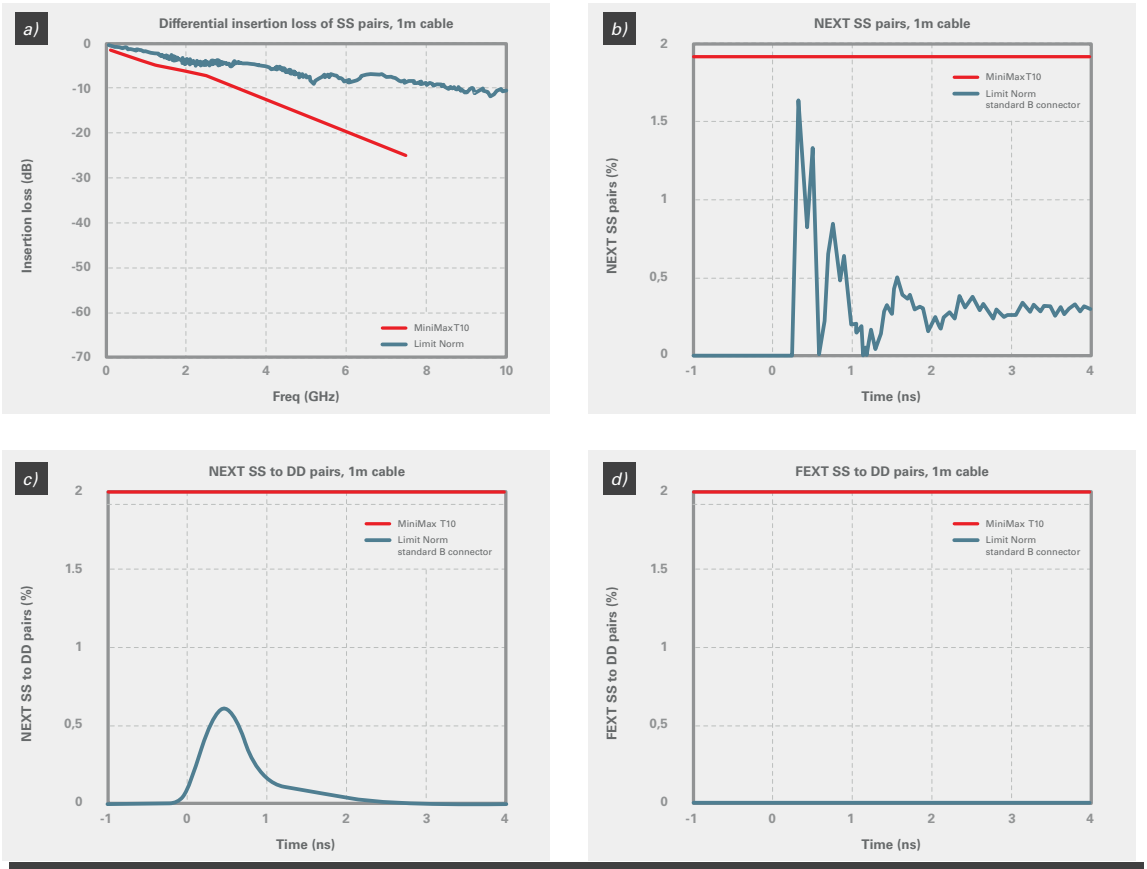


Figure 9. Examples of VNA measurement for USB 3.2 Gen 2 specifications:
a) differential insertion loss of SS pairs, b) NEXT of TX to RX, c) NEXT of SS to DD, d) FEXT of SS to DD.

SYSTEM-LEVEL TESTING (SERDES SIMULATION)

Up to this point, we have discussed the connector design challenge and how to characterize the performance of a cable-connector assembly for a required standard. However, the overall speed of a communication system on the physical layer depends on the physical layer's architecture and the specifications of the transmitter and receiver. For example, there are numerous situations in which the channel eye diagram is closed, due to high insertion loss at the receiver input without considering equalization, and the eye can easily be opened by including equalization circuits. An example of eye diagram improvement is provided in Figure 10.

FIG.10

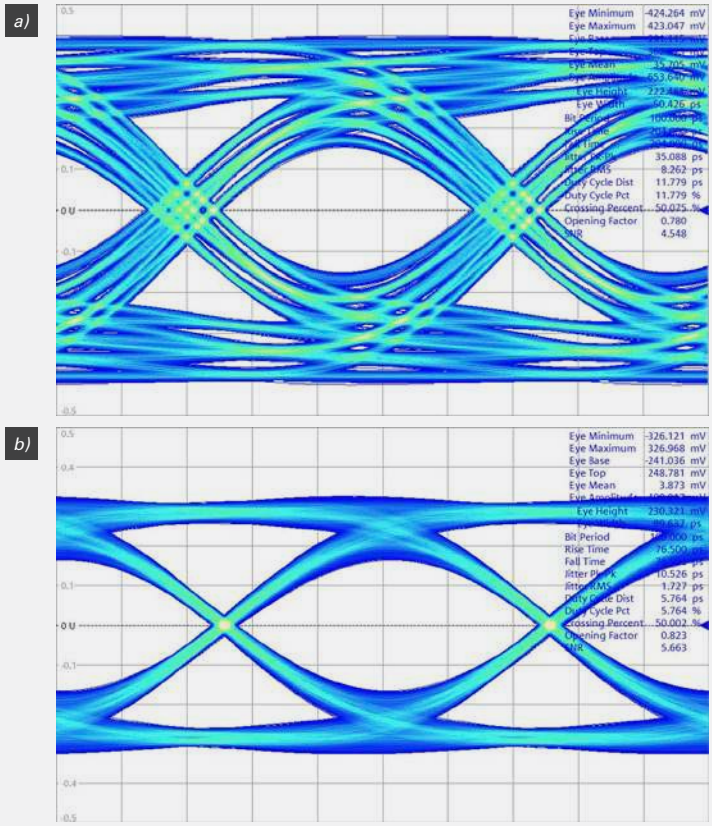


Figure 10. An example of eye improvement for 10 Gbps NRZ data: a) without EQ, b) with EQ.

Hence, including transceiver models, TX and RX buffers, TX and RX packages, Pre-emphasis, De-emphasis, equalization circuits and clock data recovery modules is essential on fully characterizing the link. To further investigate the speed of a cable-connector assembly, one can derive system-level parameters, such as eye diagrams, bathtub curves, etc.

Fortunately, IC vendors provide models of these components in IBIS-AMI formats, which can be incorporated into the cable-connector measurement via EDA tools to assess the system's overall performance.

Here we have used the tusb1310a transceiver models (provided by TEXAS Instruments Inc.) with our MiniMax T10 (shown in Figure 11) cable assembly for 5 Gbps NRZ USB 3.2 (Gen 1) communication. We drew a timing bathtub curve and statistical eye diagram. The model does not use any emphasis or equalization circuit to improve results. To make the channel more realistic, a random jitter of 0.23/(2*7.94) at BER of 1e-12 is included in the channel.

Figure 11. MiniMax T10 12 pins for USB 3.2 Gen 1 and Gen 2 applications.

FIG.12

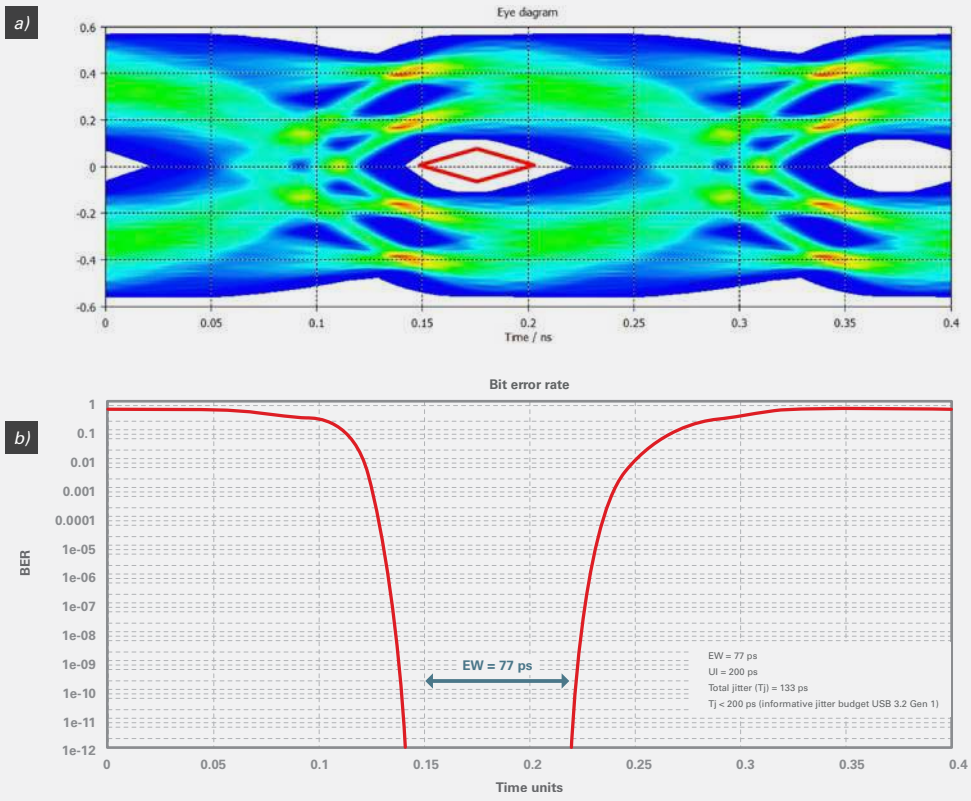


Figure 12. System-level (SERDES) simulation of MiniMax link at 5 Gbps:
a) eye diagram opening compared to Minimum Eye Opening for USB 3.2 Gen 1, b) bathtub timing curve and jitter calculations at receiver ports.

Approved performance of the channel at the required speed is demonstrated using both frequency domain measurement and SERDES simulations.

CONCLUSION

Design engineers need to optimize their products to ensure that they meet new requirements for high-speed data transmission. In this brief overview, we have discussed the connectivity challenges relating to high-speed data transmission, explaining the concept of wave propagation as opposed to conventional DC connectivity. We outline best practices in connector design. Each high-speed related design must be cross optimized for all aspects of Mechanical, Electrical, Signal Integrity, and EMI/EMC performances. There are many applications in which a special configuration of a communication link may deviate from specifications in the standards. The importance of undertaking a SERDES becomes particularly evident in such cases. We explain how to ensure that cables and connector assemblies achieve the required bit error rate (BER) needed for a reliable data transmission using SERDES simulation. Measurement and simulation examples are provided from component-level to system-level solutions.

REFERENCES

[1] Harrington, R. F., Antennas and Propagation Society & Microwave Theory and Techniques Society (1961), *Time-Harmonic Electromagnetic Fields* (Vol. 224), New York: McGraw Hill.

[2] Universal Serial Bus 3.2 Specification, https://www.usb.org

ABOUT FISCHER CONNECTORS

Fischer Connectors designs, develops, and deploys high-performance connectivity solutions that are world-renowned for their high reliability, durability and quality in harsh environments. Tested to MIL-SPEC and IEC standards, RoHS and REACH compliant, Fischer Connectors' products and solutions use the latest technologies in ruggedness, sealing, high density and data transmission, which have made the Swiss-based company the preferred supplier and global connectivity partner of leading electronic systems, device and component manufacturers worldwide for various demanding application fields such as defense & security, medical, and test & measurement.

Primary design and manufacturing facilities are located in Saint-Prex, Switzerland, with subsidiaries and distributors located worldwide.

Fischer® CONNECTORS

HEADQUARTERS
Chemin du Glapin 20
CH-1162 Saint-Prex
Switzerland
fischerconnectors.com